

TECHNICAL MANUAL

**ORGANIZATIONAL MAINTENANCE MANUAL
RADAR INTERFACE EQUIPMENT MAINTENANCE
RADAR INTEGRATION UNITS 1 AND 2**

**EXPANDED TROUBLESHOOTING
(LOGIC DIAGRAMS)**

**GUIDED MISSILE
AIR DEFENSE SYSTEM
AN/TSQ-73**

HEADQUARTERS, DEPARTMENT OF THE ARMY

4 APRIL 1985

**ORGANIZATIONAL MAINTENANCE MANUAL
RADAR INTERFACE EQUIPMENT MAINTENANCE
RADAR INTEGRATION UNITS 1 AND 2**

**EXPANDED TROUBLESHOOTING
(LOGIC DIAGRAMS)**

GUIDED MISSILE AIR DEFENSE SYSTEM

AN/TSQ-73

REPORTING OF ERRORS

You can help improve this publication. If you find any mistakes, or if you know of a way to improve the procedures, please let us know. Mail your letter, DA Form 2028 (Recommended Changes to Publications and Blank Forms), or DA Form 2028-2 located in back of this manual direct to: Commander, U.S. Army Missile Command, ATTN: AMSMI-LC-ME-P, Redstone Arsenal, AL 35898-5238. A reply will be furnished to you.

TABLE OF CONTENTS

<i>Chapter</i>		<i>Page</i>
5	LIST OF ILLUSTRATIONS.....	ii
	LIST OF TABLES.....	iii
	Section XV. RADAR INTEGRATION UNITS	
5-48	General.....	5-775
5-49	Logic Diagrams.....	5-775
5-50	Using Logic Diagrams.....	5-775

LIST OF ILLUSTRATIONS

<i>Figure</i>		<i>Page</i>
5-4	Radar Integration Unit 1A1A1A4 Bay 1, Component Location	5-775
5-5	Radar integration Unit 1A1A1A4 Bay 2, Component Location.....	5-776
FO-126	IOB Input Register and Interface Circuits Logic Diagram	
FO-127	IOB Function Commands Logic Diagram	
FO-128	IOB Parity Generation Checker Logic Diagram	
FO-129	IOB Command Control Logic Diagram	
FO-130	IOB Data Output Strobe Generator Logic Diagram	
FO-131	IOB Interrupt Register Logic Diagram.....	
FO-132	IOB I/O Logic Diagram.....	
FO-133	IOB OFR Data, Address and Clock Logic Diagram.....	
FO-134	IOB Devise Interrupt and Reset Control Logic Diagram.....	
FO-135	IOB Status 1 Error Register and Control Logic Diagram	
FO-136	IOB Status 2, 3 and 4 Error Register Logic Diagram.....	
FO-137	IOB Automatic Gate Multiplexer Logic Diagram	
FO-138	IOB Input/Output Data Multiplexer Logic Diagram	
FO-139	VDU Holding Registers Logic Diagram	
FO-140	VDU Special Video Select and IFF Decode Logic Diagram	
FO-141	VDU Video Selection and Decoding Logic Diagram.....	
FO-142	VDU Video Mixers Logic Diagram	
FO-143	RSU Special Clock Generator Logic Diagram	
FO-144	RSU Pretrigger/Range Zero Stretcher Logic Diagram.....	
FO-145	RSU Pretrigger Alignment Logic Diagram	
FO-146	RSU Range Zero/Range Max Decode Logic Diagram	
FO-147	RSU Variable Frequency Divider Logic Diagram	
FO-148	RSU Range Counter Logic Diagram.....	
FO-149	RSU Radar Clock Generator Logic Diagram.....	
FO-150	RSU TPS-32/ACM Clock Generator and Error Check Logic Diagram	
FO-151	TDU-A Timing Logic Diagram	
FO-152	TDU-B Timing Logic Diagram	
FO-153	TDU MTI and Matrix Logic Diagram	
FO-154	TDU-A Write Register Logic Diagram.....	
FO-155	TDU-B Write Register Logic Diagram.....	
FO-156	TDU RAM Address Counter Logic Diagram.....	
FO-157	TDU-A RAM Clip Selection Logic Diagram.....	
FO-158	TDU-B RAM Clip Selection Logic Diagram.....	
FO-159	TDU-B RAM Addressing and Clear Logic Diagram	
FO-160	TDU PROM Logic Diagram	
FO-161	TDU Channel A RAM Logic Diagram.....	
FO-162	TDU Channel B RAM Logic Diagram.....	
FO-163	TDU-A Start/Stop Comparators Logic Diagram	
FO-164	TDU-B Start/Stop Comparators Logic Diagram	
FO-165	TDU BITE Register Logic Diagram.....	
FO-166	SDC Interface Logic Diagram.....	
FO-167	SDC Clock Generator Circuit Logic Diagram	
FO-168	SDC Phase Logic Diagram.....	
FO-169	SDC ANP/ACP Select Logic Diagram	

LIST OF ILLUSTRATIONS (Continued)

Figure		Page
FO-170	SDC Frequency Doubler Logic Diagram.....	
FO-171	SDC BAMS Counter and Adder Logic Diagram	
FO-172	SDC ANP/ACP Logic Diagram	
FO-173	SDC Angle Mark Generator Logic Diagram	
FO-174	SDC Memory Address and Enable Logic Diagram.....	
FO-175	SDC BAMS Memory Logic Diagram.....	
FO-176	SDC Sine/Cosine Select Logic Diagram.....	
FO-177	SDC Sine Add/Subtract Logic Diagram	
FO-178	SDC Cosine Add/Subtract Logic Diagram	
FO-179	SDC Sine/Cosine Serial Output Logic Diagram	
FO-180	SDC BITE Register Logic Diagram.....	
FO-181	DIU Radar Simulator Data Selection and Control Logic Diagram.....	
FO-182	DIU Module-26 Counter Logic Diagram	
FO-183	DIU Data Receive Detector Logic Diagram	
FO-184	DIU Data Registers Logic Diagram.....	
FO-185	IIU Clock and Initialization Logic Diagram	
FO-186	IIU Range and Azimuth Compare Logic Diagram	
FO-187	IIU Mode Sequence and Gating Logic Diagram	
FO-188	IIU Adjustable Precision Time Delay Logic Diagram	
FO-189	IIU IFF Interface Circuit Logic Diagram	
FO-190	IIU Video Quantizer Logic Diagram	
FO-191	IIU Delay Lines Logic Diagram	
FO-192	IIU Emergency Decoders Logic Diagram.....	
FO-193	IIU Before and After Density PROM Logic Diagram.....	
FO-194	IIU Mode 4 Density Logic and Test Gate Generator Logic Diagram	
FO-195	IIU IFF Input Queue Logic Diagram.....	
FO-196	IIU IFF Range Comparator Logic Diagram	
FO-197	IIU Radar Range Comparator Logic Diagram	
FO-198	IIU Range and History Correlator Logic Diagram	
FO-199	IIU Memory Control Logic Diagram	
FO-200	IIU Target Start RAM Logic Diagram	
FO-201	IIU IFF Output Queue Logic Diagram	
FO-202	IIU Pulse Generator Logic Diagram	
FO-203	IIU Radar Output Queue Logic Diagram.....	
FO-204	IIU Input/Output Control Logic Diagram.....	
FO-205	IIU BITE Register and Control Logic Diagram	

LIST OF TABLES

<i>Table</i>		<i>Page</i>
5-39	Radar Integration Unit 1A1A1A4, Circuit Card Location.....	5-777
5-40	Card Pin to Test Point Correlation.....	5-786

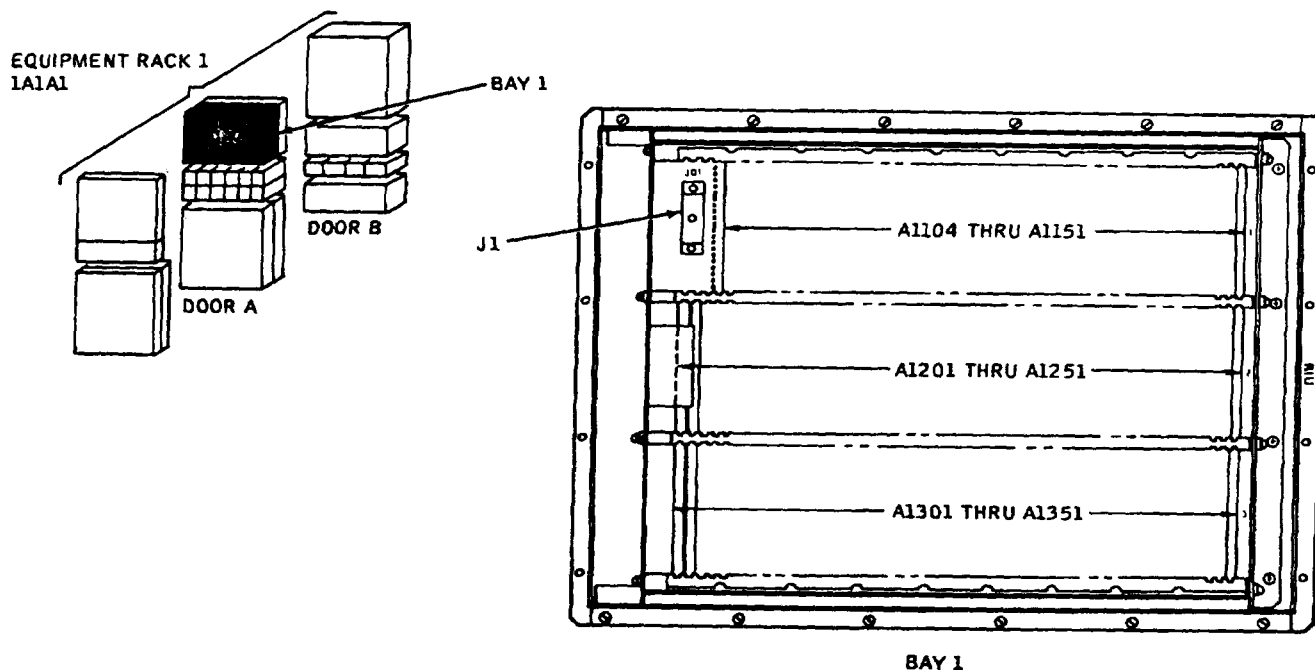
SECTION XV. RADAR INTEGRATION UNITS

5-48. General. This manual is Volume 5 of TM 9-1430-655-20-3, Radar Interface Equipment Maintenance for Guided Missile Air Defense System AN/TSQ-73. It contains the logic diagrams covering radar integration units (RIU) 1 and 2 for use and guidance of advanced personnel responsible for repair of the RIE. Foldouts 126 through 165 cover RIU 1 and foldouts 166 through 205 cover RIU 2. RIU 1 and 2 are located in equipment rack 1, 1A1A1, door A, in two card cage bays. Figure 5-4 illustrates bay 1 and figure 5-5 illustrates bay 2.

5-49. Logic Diagrams. Logic diagrams provide the maintenance technician pin to pin signal flow, traceable by signal mnemonics and I/O tables, to help identify faulty cards and to troubleshoot faults in the backplane

wiring and other areas that are beyond fault isolation capabilities of the MTS.

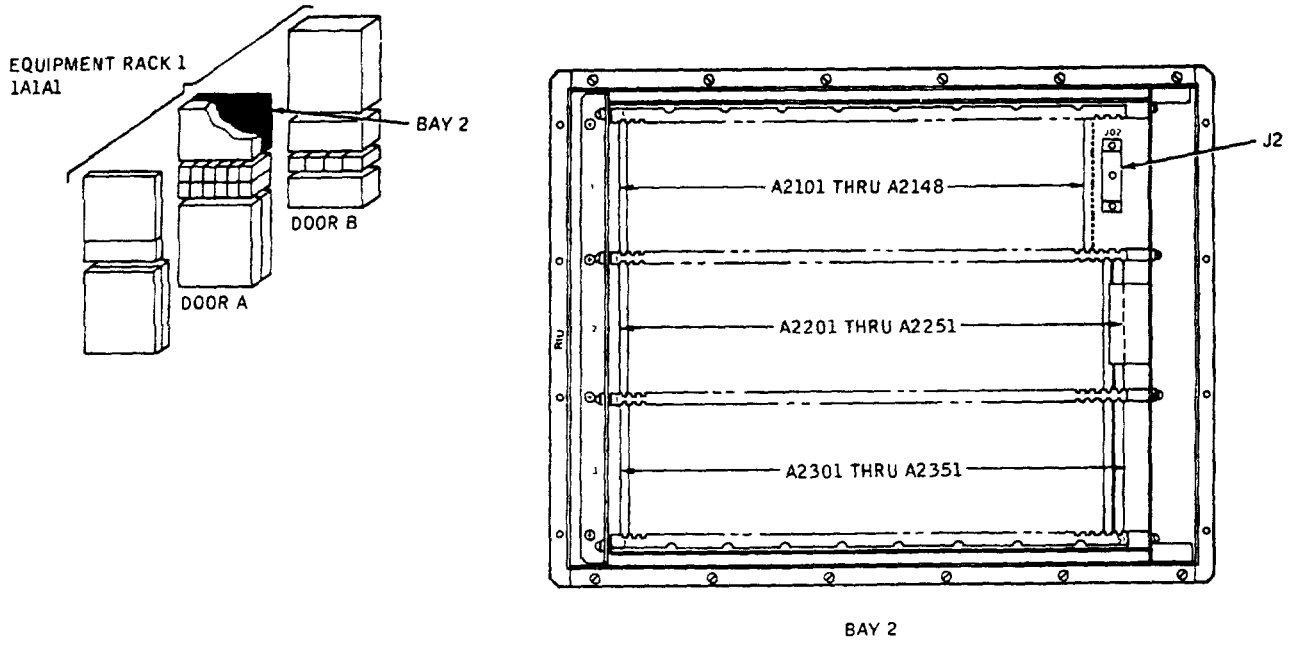
5-50. Using Logic Diagrams. Logic diagrams in this manual show signal flow in functional subsystems of RIU 1 and 2. Signal flow is traceable between circuit card pin numbers and is shown as inputs and outputs of integrated circuit logic devices on the circuit card. A specific signal can be followed between foldouts by using the signal mnemonic and the logic diagram input/output table. The circuit card slot is shown within the integrated circuit card device symbol. Table 5-39 contains the circuit card slot and the part number of the card. Table 5-40 contains, by card part number, the test point for each of the 80 pins of MTS testable cards.



MS 197185

Figure 5-4. Radar Integration Unit 1A1A1A4 Bay 1, Component Location

Change 1 5-775



MS 197186

Figure 5-5. Radar Integration Unit 1A1A1A4 Bay 2, Component Location

Table 5-39. Radar Integration Unit 1A1A1A4, Circuit Card Location

Card slot	Part number	Card type	Color code			
			1	2	3	4
BAY 1-SHELF 1						
A1101	-	-	-	-	-	-
A1102	-	-	-	-	-	-
A1102	-	-	-	-	-	-
A1103	-	-	-	-	-	-
A1104	W308	Connector	-	-	-	-
A1105	W309	Connector	-	-	-	-
A1106	W528	Connector	-	-	-	-
A1107	W529	Connector	-	-	-	-
A108	587104-102	Dual 4-input NAND gate	-	-	Yellow	-
A109	587104-102	Dual 4-input NAND gate	-	-	Yellow	-
A110	587104-102	Dual 4-input NAND gate	-	-	Yellow	-
A111	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1112	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1113	587100-102	4/8 MHz oscillator	-	-	-	-
A1114	10281652	3-input J-K flip-flop	Brown	Blue	Green	Red
A1115	10281652	3-input J-K flip-flop	Brown	Blue	Green	Red
A1116	10281652	3-input J-K flip-flop	Brown	Blue	Green	Red
A1117	10281652	3-input J-K flip-flop	Brown	Blue	Green	Red
A1118	10281652	3-input J-K flip-flop	Brown	Blue	Green	Red
A1119	587102-102	Quad 2-input NAND gate	-	-	-	Red
A1120	587102-102	Quad 2-input NAND gate	-	-	-	Red
A1121	10281606	Hex 4-bit shift register	Brown	Blue	Black	Blue
A1122	10281606	Hex 4-bit shift register	Brown	Blue	Black	Blue
A1123	587119-100	240-ohm resistor	-	-	-	-
A1124	587108-102	Single 8-input NAND gate	-	-	Gray	-
A11251	10281610	Hex 4-bit comparator	Brown	Blue	Brown	Black
A1126	10281609	Quint 4-bit adder	Brown	Blue	Black	White
A1127	10281609	Quint 4-bit adder	Brown	Blue	Black	White
A1128	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1129	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1130	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1131	587102-102	Quad 2-input NAND gate	-	-	Red	-
A11321	587104-102	Dual 4-input NAND gate	-	-	Yellow	-
A1133	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1134	587102-102	Quad 2-input NAND gate	-	-	Red	-

See footnote at end of table.