

TECHNICAL MANUAL

**ORGANIZATIONAL MAINTENANCE MANUAL
DISPLAY EQUIPMENT MAINTENANCE**

**EXPANDED TROUBLESHOOTING
(LOGIC DIAGRAMS)**

**GUIDED MISSILE AIR DEFENSE SYSTEM
AN/TSQ-73**

**HEADQUARTERS, DEPARTMENT OF THE ARMY
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ORGANIZATIONAL MAINTENANCE MANUAL: DISPLAY EQUIPMENT MAINTENANCE
EXPANDED TROUBLESHOOTING (LOGIC DIAGRAMS) .
GUIDED MISSILE AIR DEFENSE SYSTEM AN/TSQ-73

REPORTING ERRORS AND RECOMMENDING IMPROVEMENTS

You can help improve this manual. If you find any mistakes, or if you know of a way to improve the procedures, please let us know. Mail your letter, DA Form 2028 (Recommended Changes to Publications and Blank Forms) or DA Form 2028-2, located in back of this manual, direct to: Commander, U.S. Army Missile Command, ATTN: AMSMI-LC-ME-P, Redstone Arsenal, AL 35898-5238. A reply will be furnished to you.

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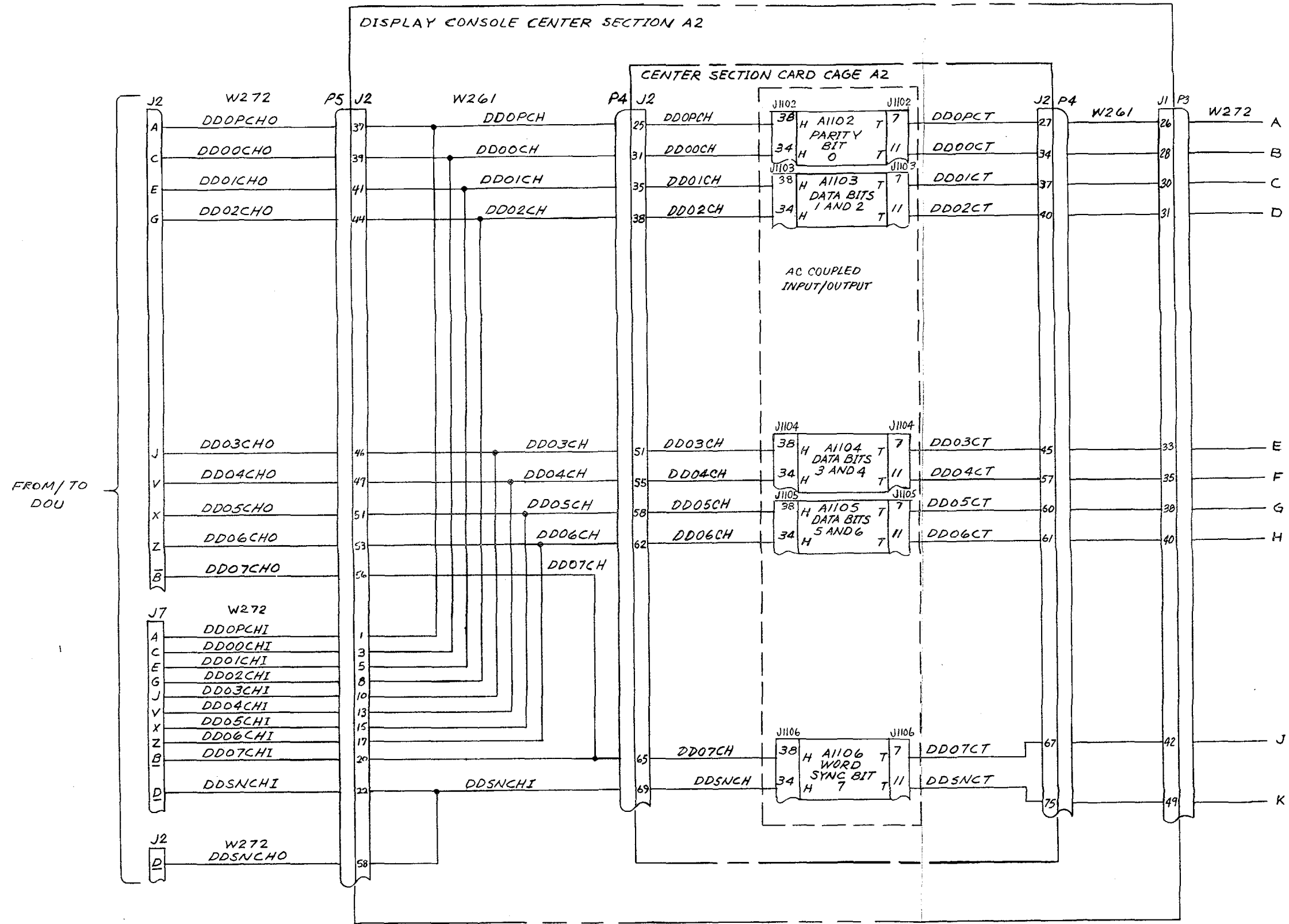
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DISPLAY CONSOLE CENTER SECTION A2

CENTER SECTION CARD CAGE A2

- NOTES: UNLESS OTHERWISE SPECIFIED
- PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATIONS, PREFIX WITH APPLICABLE UNIT NUMBER AND ASSEMBLY DESIGNATION.
 - ALL CIRCUITS SHOWN ON THIS FIGURE ARE CONTAINED ON LEFT HAND CARD CAGE A1A1. (SINCE MULTIPLE DISPLAY CONSOLES ARE SHOWN), ABBREVIATED DESIGNATIONS ARE USED.
 - DEFINITIONS FOR SYMBOLS SHOWN ARE AS FOLLOWS:
 - ▲ INPUT FROM ANOTHER FIGURE
 - △ INPUT FROM SAME FIGURE
 - OUTPUT TO ANOTHER FIGURE
 - ◻ OUTPUT TO BOTH SAME AND ANOTHER FIGURE
 - OUTPUT TO SAME FIGURE
 - REFER TO TABLE 5-3 THRU 5-5 FOR CIRCUIT CARDS THAT ARE MODULE TEST SET TESTABLE AND CIRCUIT CARD LOCATIONS.
 - REFER TO TABLE 5-6 THRU 5-8 FOR COMPLETE SIGNAL LOOK UP AND CIRCUIT CARD TEST POINTS.
 - REFER TO DISPLAY CONSOLE POWER DISTRIBUTION DIAGRAMS FOR DC POWER AND GROUND CIRCUITS.
 - CIRCUIT SYMBOLS INCLUDE CARD LOCATIONS AND CIRCUIT CARD PIN NUMBERS.
 - SP1XXX INDICATES +5V PULL UP THROUGH RESISTOR CARDS; REFER TO TABLE 5-6 THRU 5-8 FOR COMMON LISTING.



INPUTS	F/O - SH	OUTPUTS	F/O - SH
A10MA04	54-2	ADDDT0	4-1
ABLTC2E	4-1	ADDFBR	4-1
ADDBL0	4-1	ADDFB8	4-1
AIBR8D4	53-0	ADDL0R	2-0
LADR80	53-0	ADDL1R	2-0
LIBENA	51-0	ADDL2R	2-0
LJBPFJ	49-0	ADDL3R	2-0
LMMAN8	49-0	ADDL4R	2-0
LTSAG2E	48-1	ADDL5R	2-0
LTBCG0E	48-1	ADDL6R	2-0
LTBCG1E	48-1	ADDL7R	2-0
LTBCG2E	48-1	ADMFTA	2-0
LTBCG3E	48-1		
LTBDG0E	48-1		
LTBDG1E	48-1		
LTBDG2E	48-1		
LTBDG3E	48-1		

FO-1. Alterable Processor High Speed Input Buffer Input Logic Diagram (Sheet 1 of 2)